EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S95	1272	716/2.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 10:02
S96	122672	threshold adj2 voltage	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 10:06
S97	106	S95 and S96	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 10:10
S100	2535	(hybrid mix$3 multi) with (threshold adj2 voltage LVT RVT)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:04
S101	837	(LSSD level adj sensitive adj scan adj design) with (ff flip-flop register latch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:06
S103	1	S100 and S101	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:09
S104	140	S100 and S102	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:10
S105	324	S101 and S102	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:10

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S106	1	S104 and S105	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:10
S107	697	(level adj sensitive) near4 (latch ff register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:11
S108	1	S104 and S107	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:12
S109	96	S105 and S107	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 11:13
S110	1446	716/1.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:02
S113	80	threshold adj voltage and ((level adj sensitive adj scan) near4 (ff register latch) or LSSD)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:36
S114	13	S110 and S113	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:37
S115	0	(latch ff register flip-flop) and ((level adj sensitive adj scan adj device) or LSSD) and logic adj block and critical same path and ("L1" or "L2" level adj ("1" or "2")) and (threshold adj voltage LVT HVT RVT) and implement$3 and scan$4 adj2 (signal input)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:47

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S116	0	((latch ff register flip-flop) and ((level adj sensitive adj scan adj device) or LSSD) and logic adj block and critical same path and ("L1" or "L2" level adj ("1" or "2")) and (threshold adj voltage LVT HVT RVT) and implement$3 and scan$4 adj2 (signal input)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:48
S117	19966	implement$3 and (Q quiescent adj power adj dissipation) and threshold and (mixed multi hybrid)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:52
S119	1253	(latch ff flip-flop register) same (LSSD level adj sensitive adj scan)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:58
S120	10	S117 and S119	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 18:58
S102	276789	"L1" or "L2" or (stage level) adj2 ("1" or "2") near4 (ff flip-flop register latch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:00
S121	276789	"L1" or "L2" or (stage level) adj2 ("1" or "2") near4 (ff flip-flop register latch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:00
S122	1491	(level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:21
S123	122	(level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register) and critical near4 path	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:21

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S124	64	(level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register) and critical same path same clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:22
S126	2	(level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register) and critical same path same clock and ("L1" or "L2" level adj ("1" or "2")) and ((low high) adj threshold LVT RVT LLD low adj leakage)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:25
S127	0	((level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register) and critical same path same clock and ("L1" or "L2" level adj ("1" or "2")) and ((low high) adj threshold LVT RVT LLD low adj leakage)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:25
S125	31	(level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register) and critical same path same clock and ("L1" or "L2" level adj ("1" or "2"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:28
S128	38	(level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register) and critical same path same clock and ("L1" or "L2" (stage level) near3 ("1" or "2"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:32
S129	33	(level adj2 sensitive adj2 scan LSSD) and (latch ff flip-flop register) and critical and non-critical and path and clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:35
S130	771866	"L1" or "L2" or (stage or level) near3 ("1" or "2")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:36
S131	28	S129 and S130	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:38

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S132	221	(LVT low adj voltage adj threshold) with transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:39
S133	2	S131 and S132	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/20 19:39